INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet 1 of 1

Complete if Known	
Application Number	10/816,144
Filing Date	March 31, 2004
First Named Inventor	Ulrich Bortfeld
Art Unit	2186
Examiner Name	Lev Iwashko
Attorney Docket Number	42P19079

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
LI		RAMINDER S. BAJWA ET AL., "Instruction Buffering to Reduce Power in Processors for Signal Processing", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 5, No. 4, December 1997, pg. 417-424.	
LI		PAUL WANG LEE, "Trace Cache", EE482: Advanced Computer Organization, Lecture #5, Processor Architecture, *Stanford University*, May 10, 2000, pg. 1-4.	
LI		PAUL W. LEE, "Exploring the Trace Cache Design Space", EE482a - Prof. William Dally, *Stanford University*, May 30, 2000, pg. 1-14.	
LI		CHANGWOO JUNG ET AL., "Instruction Cache Organisation for Embedded Low-Power Processors", *Electronics Letters*, Vol. 37, No. 9, April 26, 2001, pg. 554-555.	

Examiner Signature	/Lev Iwashko/	Date Considered	08/22/2006

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

[1]Applicant's unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.